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# Microcontact patterning of ruthenium gate electrodes by selective area atomic layer deposition

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Patterned octadecyltrichlorosilane monolayers are used to inhibit film nucleation, enabling selective area atomic layer deposition (ALD) of ruthenium on $SiO_2$ and $HfO_2$ surfaces using bis-(cyclopentadienyl)ruthenium and oxygen. X-ray photoelectron spectroscopy indicated that OTS could deactivate film growth on thermal silicon oxide and hafnium oxide surfaces. The growth rate of ALD Ru is similar on various starting surfaces, but the growth initiation differed substantially. Metal-oxide-semiconductor capacitors were fabricated directly using the selective-area process. Capacitance measurements indicate the effective work function of ALD Ru is $4.84 \pm 0.1$ eV on $SiO_2$, and the effective work function is reduced on $HfO_2/SiO_2$ layers. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1852079]

Improved control of interface reactions during thin film processing is critical for advanced electronic and optical devices. Ruthenium is of interest for advanced metal/oxide/semiconductor (MOS) transistor gate electrodes to reduce polysilicon depletion effects and as nucleation layer for copper interconnect layers.[1] Ruthenium is considered a viable candidate for *p*-type MOS devices because it has a vacuum work function near the conduction band edge of silicon, good thermal stability, and low resistivity of the oxidation phase.[2]

Microcontact-printed organic monolayer resists have previously been used for selective area atomic layer deposition (ALD) of oxides[3–5] and for chemical vapor deposition (CVD) of metals.[6] A previous report demonstrates selective area digital CVD Ru using patterned photoresist.[7] In this work, selective deposition of Ru is demonstrated using contact printed self-assembled monolayer resists by ALD processing. Also in this work, spectroscopic characterization is used to demonstrate selectivity, and the effect of processing on the monolayer structure is analyzed. Selective deposition enables direct formation of $Ru/HfO_2(SiO_2)/Si$ capacitor stacks, and the effective work function of ALD Ru is characterized on $HfO_2$ and $SiO_2$ dielectrics. A key problem for metals in CMOS is methodology to enable integration of two different metal work functions. Techniques to integrate two different metals in nanoscale device fabrication include selective modification of a metal, for example by interdiffusion[8,9] or by silicide formation,[10] or by metal alloy formation.[11] We suggest here that selective area ALD is a possible alternate route to dual-metal gate integration.

ALD Ru was carried out in a home-built hot-wall quartz tube reactor using $RuCp_2$ [bis-(cyclopentadienyl)ruthenium] as a precursor and dry oxygen. $RuCp_2$ is solid at room temperature with vapor pressure of ~10 mTorr at the bubbler temperature of 80 °C. To prepare substrates, silicon surfaces were oxidized by wet chemical treatment (BakerClean® JTB-100), followed by buffered HF acid dip, deionized water rinse, and $N_2$ flow dry. Silicon was either directly oxidized to form $SiO_2$, (900 °C in air) or coated with thin Hf films by sputtering, followed by thermal oxidation. For example, the Hf based films with equivalent oxide thickness (EOT) of 30 Å consisted of 11 Å of sputtered hafnium followed by oxidized in $N_2$ (with ~20 ppm $O_2$) at 600 °C for 1 min.[12] These conditions likely resulted in growth of $HfO_2$ with some interfacial $HfSiO_x$ and/or $SiO_2$. The samples are referred to here as $HfO_2/SiO_2$ films.

To prepare the patterned organic monolayer an elastomeric stamp was made of polydimethylsiloxane (PDMS) solution and a curing agent. The mold patterns for the PDMS stamps were micron-scale line/space photoresist and metallic dots made by physical vapor deposition of aluminum through a shadow mask. A solution of OTS (octadecyltrichlorosilane) in dry hexane (10 mM) was used as the "ink." The OTS solution was applied to the PDMS stamp by spin coating, and the inked stamp was dried in nitrogen flow for 30 s. The stamp was then brought into contact with the clean substrate and held in place for 30–60 s. The resulting OTS films were characterized by water contact angle analysis, scanning force microscopy, and x-ray photoelectron spectroscopy (XPS). For some measurements, OTS was also deposited by directly exposing the oxidized silicon to its solution at room temperature. Resulting films showed a static contact angle with water to be between $<90$ and 110°, consistent with a range of film quality, from relatively poorly packed ($<90°$), to highly packed (110°) films.[13,14] Films with contact angle $\geqslant 90°$ show similar results in inhibiting deposition. After exposure to 300 cycles of Ru ALD, the OTS monolayers generally showed reduced contact angle ($<80°$), indicating monolayer degradation. The results suggest that Ru nucleation is not as sensitive to quality of the monolayer surface as observed for Hf or Zr oxide[15] and Ti based[13] film deposition. This may be due to the higher oxygen affinity of Hf, Zr, and Ti where these metals are more likely to penetrate the monolayer and react with oxide present at the Si/monolayer interface.

The OTS-patterned substrates were rinsed in hexane and deionized water, then dried with nitrogen flow before being loaded into the ALD reactor. The ALD chamber was evacuated to $5 \times 10^{-6}$ Torr, and the precursor and oxidant gases were introduced into the reactor in separate pulses (3 and 6 s,

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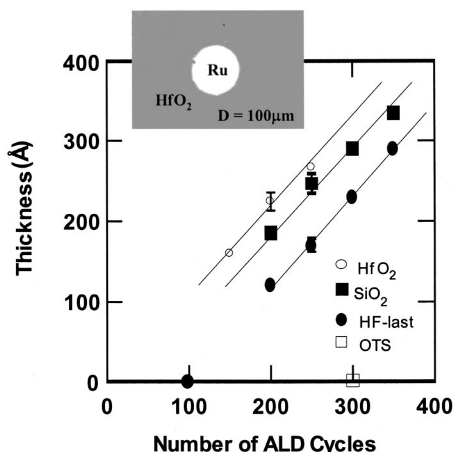


FIG. 1. Ruthenium film thickness vs number of ALD cycles as deposited on $HfO_2$, $SiO_2$, and Si–H (HF-last) surfaces, compared to deposition on OTS covered substrate. The data point at zero thickness for growth on Si–H is determined from visual inspection. The data point at zero thickness for growth on OTS is determined from XPS. Visual inspection shows clear selectivity on OTS for all conditions studied (up to 300 cycles). The error bar for each substrate represents typical measurement error (±5%) of profilometer. The inset shows an optical image of a selectively deposited Ru (100 μm diameter) metal on $HfO_2$.

respectively) with a 20 s Ar purge between each reactant. Argon was also used as a carrier gas for the $RuCp_2$ pulse. During the deposition, the total gas flow rate was constant at 100 sccm, and the chamber was dynamically pumped to maintain pressure at 1.2 Torr. Under these conditions, self limiting growth was observed at temperatures between ~310° and 350 °C corresponding to ~1 Å per deposition cycle, which is larger that 0.5 Å/cycle reported previously for Ru ALD.[16] This difference is under investigation. The resulting Ru films were characterized by surface profilometry to determine thickness, and XPS was used to determine the film chemical composition. Capacitance versus voltage (*C*–*V*) was measured using an HP 4284A LCR meter at 1 MHz using *p*-type silicon substrates with doping levels of $1.5 \times 10^{18}$ $cm^{-3}$.

Figure 1 shows Ru film thickness versus number of ALD cycles for deposition on $HfO_2/SiO_2$, $SiO_2$, and hydrogen-terminated silicon (HF last) surfaces. For deposition on the Si–H surface, no film was observed by eye after 100 cycles for the conditions used. Also, on the OTS surface, no film was observed by XPS (*vide infra*) for up to 300 cycles studied. The inset in Fig. 1 is an optical image of a selectively deposited Ru capacitor on $HfO_2/SiO_2$ using the OTS monolayer resist. The deposited thickness per cycle was similar on $SiO_2$, $HfO_2/SiO_2$, and Si–H, but the intercepts show different values, consistent with different incubation times for growth on these surfaces. However, details of growth incubation require more investigation of thin (<100 Å) layer growth.[17] Figures 2(a) and 2(b) show XPS spectra after 150 cycles of selective ALD Ru at 325 °C on clean $SiO_2$ and on $SiO_2$ covered with microcontact-stamped OTS. Figure 2(b) shows that the Ru 3*p* peaks are not observed on the OTS covered regions after ALD, indicating good selectivity to Ru growth with this monolayer surface (static contact angle for this sample was 92° before Ru deposition). The measured Ru $3p^{1/2}$ and $3p^{3/2}$ peak positions at 484 and 462 eV, and the width of the peaks are consistent[18] with the presence of several Ru oxidation states from elemental Ru to mildly oxidized $RuO_x$. Presence of $RuO_x$ is confirmed by the existence of the O 1*s* peak, although it is possible that most of the O in confined to the surface. Because of overlap of C 1*s* and Ru 3*d* peaks, it is difficult to calibrate the XP spectrum energy scale to compensate for surface charge. The spectrum from the Ru film shows a small signal from the Si substrate peak at 98.7 eV, close to the expected value of 99.3 eV.

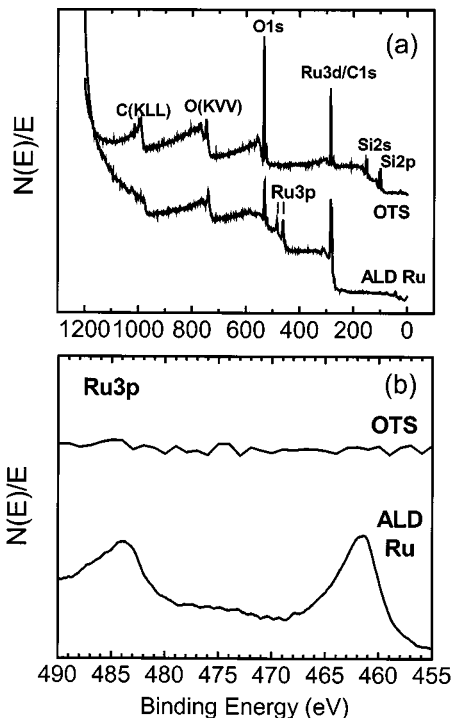


FIG. 2. (a) Survey scan, and (b) Ru 3*p* region from XPS analysis of a $SiO_2$ partially covered with OTS after 150 Ru ALD cycles at 325 °C; OTS: region with OTS covered, ALD Ru: Ru covered after on $HfO_2$ and $SiO_2$ compared to deposition on OTS covered substrate.

Figure 3(a) shows *C*–*V* characteristics of capacitors formed using selective area Ru deposition. For comparison, some capacitors [shown in Fig. 3(b)] were formed using blanket Ru followed by sputtered Al through a shadow mask and Ru dry etching. Before measurement, all capacitors received a post-metal anneal consisting of $N_2:H_2=10:1$ at 400 °C for 30 min. The *C*–*V* behavior of the selective ALD Ru capacitor shows a flatband voltage ($V_{FB}$) of −0.2 V and equivalent oxide thickness of 30 Å as determined using the Hauser *C*–*V* fitting procedure.[19] For the sputtered Al/ALD Ru capacitor, $V_{FB}$ is −1.5 V, consistent with a larger concentration of positive fixed charge in the dielectric induced by the Al sputter process that is not completely removed by the post-metal anneal.

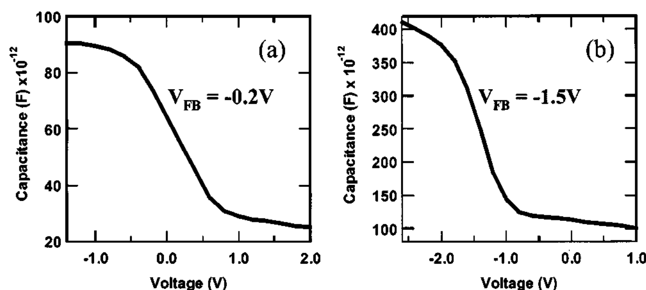


FIG. 3. Capacitance–voltage behaviors of MOS capacitors: (a) selectively deposited ALD Ru MOS; (b) conventionally processed MOS.

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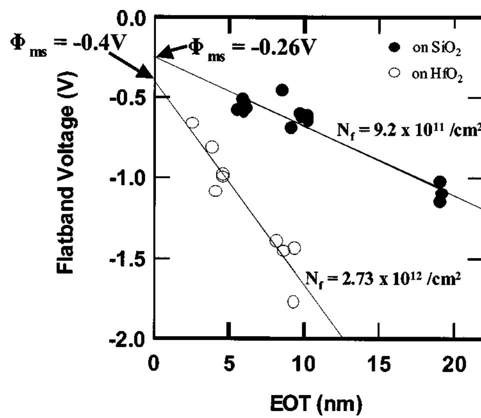


FIG. 4. $V_{FB}$ vs EOT for Ru/$SiO_2$/Si and Ru/$HfO_2$/Si capacitors. Quality of fittings ($R$): 0.9, the doping density of $p$-type Si: $1.5\times10^{18}/cm^3$, $\phi_{ms}$: the work function difference between metal and silicon substrate.

A key question for advanced gate metals is the effective work function in a capacitor structure. The $C$–$V$ curves were analyzed for a range of dielectric film thickness, and the results of $V_{FB}$ vs EOT are shown in Fig. 4. For the $HfO_2$/$SiO_2$ samples, determination of the effective work function ($\phi_{eff}$) from $C$–$V$ data must consider the effect of charge at the $SiO_2$/Si interface, as well as charge at any internal interface in the dielectric stack.[20] The data presented in Fig. 4 are not sufficient to unambiguously differentiate these interface charge densities, but the linear fit indicates that the bulk charge is relatively small in these films. For the case of Ru on $SiO_2$, the intercept $\phi_{ms}=\phi_{eff}-\phi_s$ where $\phi_s$ is the semiconductor work function. In this case, $\phi_{eff}$ is determined to be $4.84\pm0.1$ eV. The slope shows a high positive charge density at the Si/$SiO_2$ interface. The more negative intercept for Ru on $HfO_2$/$SiO_2$ is suggests a somewhat smaller $\phi_{eff}$ at the ($HfO_2$)/Ru interface, which is consistent with a different interface dipole due to differences in dielectric screening and charge neutrality levels in $SiO_2$ and $HfO_2$.[21,22] For the Ru films reported here, Auger analysis indicates O/Ru ratio of ~3% and resistivity values ranged from 35 to 20 $\mu\Omega$ cm. An effective work function of 5.1 eV has been reported for CVD Ru on $HfO_2$, where the Ru contains a higher concentration of oxygen.[7]

Another problem with metal gate integration in complementary MOS technology is the potential need for two different metal gate materials for adjacent $n$- and $p$-type MOS transistors. Processes that can selectively place one metal on a predetermined area of a substrate may provide a possible route to dual metal gate processing, to eliminate the need for a potentially damaging metal etch step. Alternate passivating approaches, beyond the OTS monolayer demonstrated here, would be helpful to further simplify processing requirements.

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